TB-FMCL-HDMI
Hardware User Manual

Rev.3.00

(For hardware revision 3.0)

Revision History

Version	Date	Description	Publisher
Rev.0.01	2010/03/02	Beta version release	Tecchikawahara
Rev.1.00	2010/04/05	Release version	Yoshioka
Rev.1.01	2010/05/27	2. Overview : Add notice of ADV7441A Table 8-1 : LED function modified Table 8-2 : Switch function modified Table 9-1 : FPGA Ping assign modified Table 11-2 : Default setting of DIP SW modified 12. Example of use : Add comment	Yoshioka
Rev1.02	2010/05/28	Table 9-1 : Changed Ping assign	Yoshioka
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Rev.1.04	2010/06/16	Table 9-1 : Changed Ping assign	Yoshioka
Rev.1.05	2010/06/24	Modified disclaimer Modified Table 8-1 LEDs Modified Table 8-2 Switches Added Figure 8-1 S1-3 is ON of connection Added Figure 8-2 S1-3 is OFF of connection Modified Table 11-2 Default settings	Yoshioka
Rev.1.06	2010/07/01	Modified disclaimer Modified related document and accessories Modified Figure 5-1, 5-2 Overview Modified Table 7-4 SCL,SDA settings Modified Table 8-2 SW Operation Added Figure 8-1, -2 Cable connections Modified Figure 11-1 Default switch settings Modified Table 11-1 Default Jumper settings Modified Table 11-2 Default DIP switch settings Modified Figure 12-1 Example of use	Yoshioka
Rev.1.07	2010/07/24	Added Figure 8-1 S1-3 is ON of connection Added Figure 8-2 S1-3 is OFF of connection	Yoshioka
Rev.1.08	2010/10/19	Modified Table 7-1 VCCIO_SEL Jumper Setting Modified Table 9-1 FPGA Pin Assignment Modified Table 11-1 Default Jumper Settings Modified Figure 12-1 Example of Use	Yoshioka
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Rev.3.00	2011/3/3	PCB version3.xx FPGA version 3.xx Modified 2. Overview Figure 4-1 Block Diagrams 7.2 HDMI Encoder block => HDMI Transmitter Block Table 7-2 HDMI connector(Transmitter side) 7.3 HDMI Decoder block => HDMI Receiver Block Table 7-3 HDMI connector(Receiver side) 7.5 Other Interfaces Table 8-1 LEDs Table 8-2 Switches Figure 8-1,2,3,4 TB-FMCL-HDMI connections Table 11-1 Initial setting(JP) Table 11-2 Initial setting(DIPSW) 12. Example of Use 13. Others	Yoshioka

Table of Contents

List of Figures

List of Tables

Introduction

Thank you for purchasing the **TB-FMCL-HDMI** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you, other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure safe use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with property if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact technical support.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates at high speed, do not put your hand close to it or touch it. Otherwise, it may cause injury.
	**Do not place the product in an unstable position.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash on it.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may be damaged and break down or it may cause a fire or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	**Do not use or place the product in the following locations.** • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Static locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	**Do not place heavy things on the product.** Otherwise, the product may be damaged.

■ Disclaimer

This product is intended for use simultaneously as a High Definition Multimedia Interface (HDMI) receiver and as an HDMI transmitter. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification
(4) Damage by connections which do not meet the following conditions:
    - Do not input video source, when this product is not powered on.
    - Do not connect/disconnect when this product is powered on.
    - Do not misconnect Input to output or output to input.

This product has been developed for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.
Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.
The specification of this product is subject to change without prior notice.
The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from the TED website (https://www.teldevice.co.jp/ppg/cgi-bin/HotLine/swTopEng.cgi/indexEng.htm). Please see attached paper on the products.

Board accessories:

- FMC spacer set
  Spacer: 4 (Large 2, small 2)
  Screws: 6
- Jumper socket set
  Jumper socket: 5

FPGA Bitstream:

- Version 2.0 goes with board revision 3.0

2. Overview

This board provides HDMI receive and transmit functions. It uses the Samtec FMC connector (Low-Pin Count) and Molex HDMI connectors. The board is designed for connection with the platform board (for example the TB-6S-LX150T-IMG) with a Low-Pin Count connector.

Notice: 1) This board uses Analog Devices Inc, ADV7441A (Encoder) and ADV7510 (Decoder).
These devices do not support High-bandwidth Digital Content Protection (HDCP) functions.
2) The ADV7441A (Encoder) is capable of accepting 8 or 12-bits per pixel input videobut the output format is 8 or 10-bits per pixel due to the FPGA to ADV7441A interface width limitation of 10-bits/color.
When receiving a 12-bit input signal, the output is reduced to 10bits (LSB 2-bits dropped).

3. Features

FMC Connector: Samtec FMC (Low-Pin Count) connector
HDMI Connector: Molex 5002541927
Power Selection: Supply voltage is selectable using an onboard jumper switch

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 3-1 FMC Connector Pinout

4. Block Diagram

Figure 4-1 shows the block diagram of the TB-FMCL-HDMI FPGA Mezzanine Card (FMC). The Samtec FMC connector is mounted on the solder side of the board.

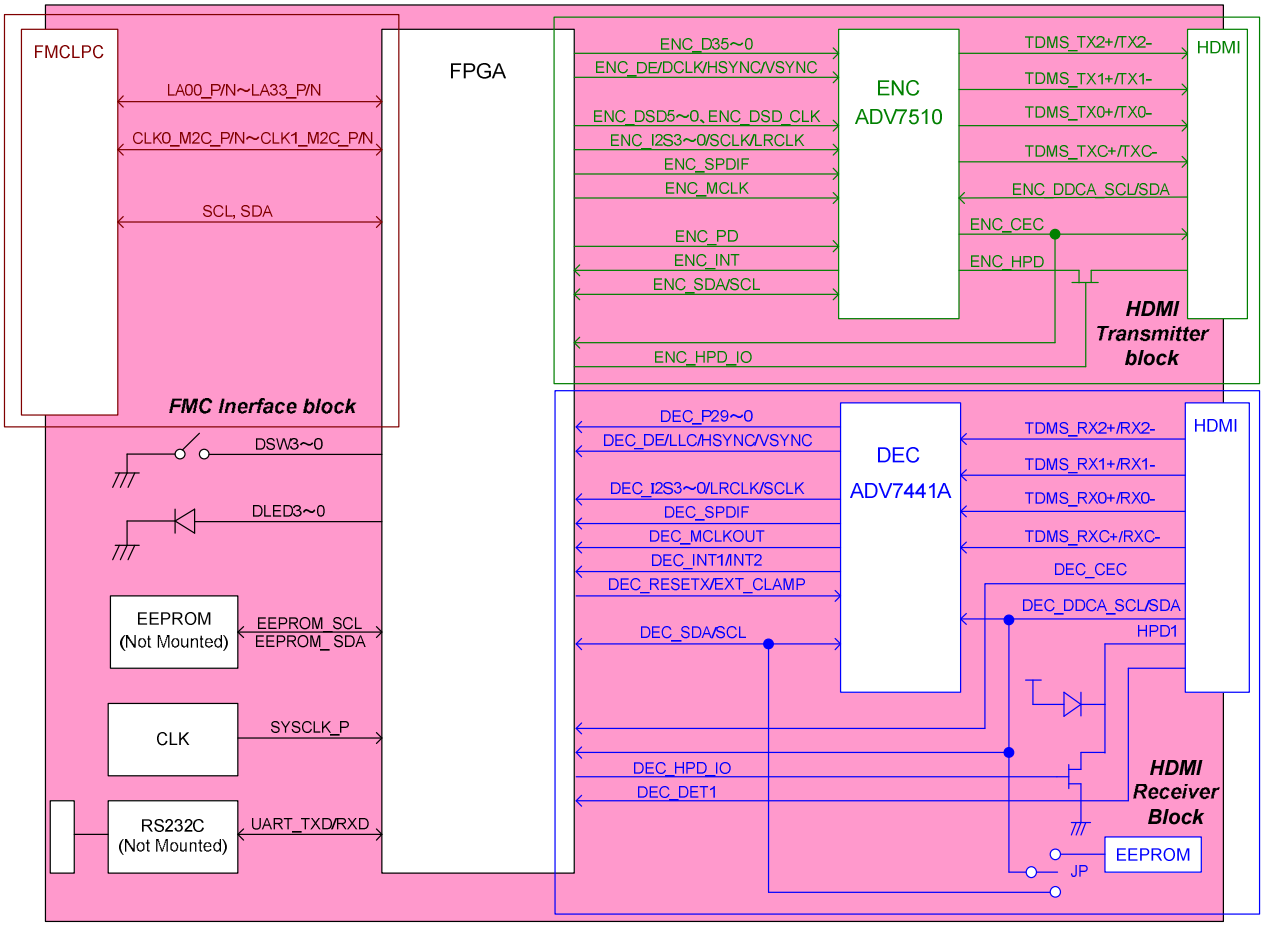

Figure 4-1 Block Diagram

Primary Interfaces:

1. HDMI Receive Function (FMC Connector to ADV7441A)
2. HDMI Transmit Function (ADV7510 to FMC Connector)
3. FMC Connector Interface (FMC Connector and FPGA)
4. JTAG Interface
5. General-Purpose Clock Interface
6. General-Purpose Switch
7. General-Purpose LED

5. External View of the Board

The following figures show the top and bottom views of the board.

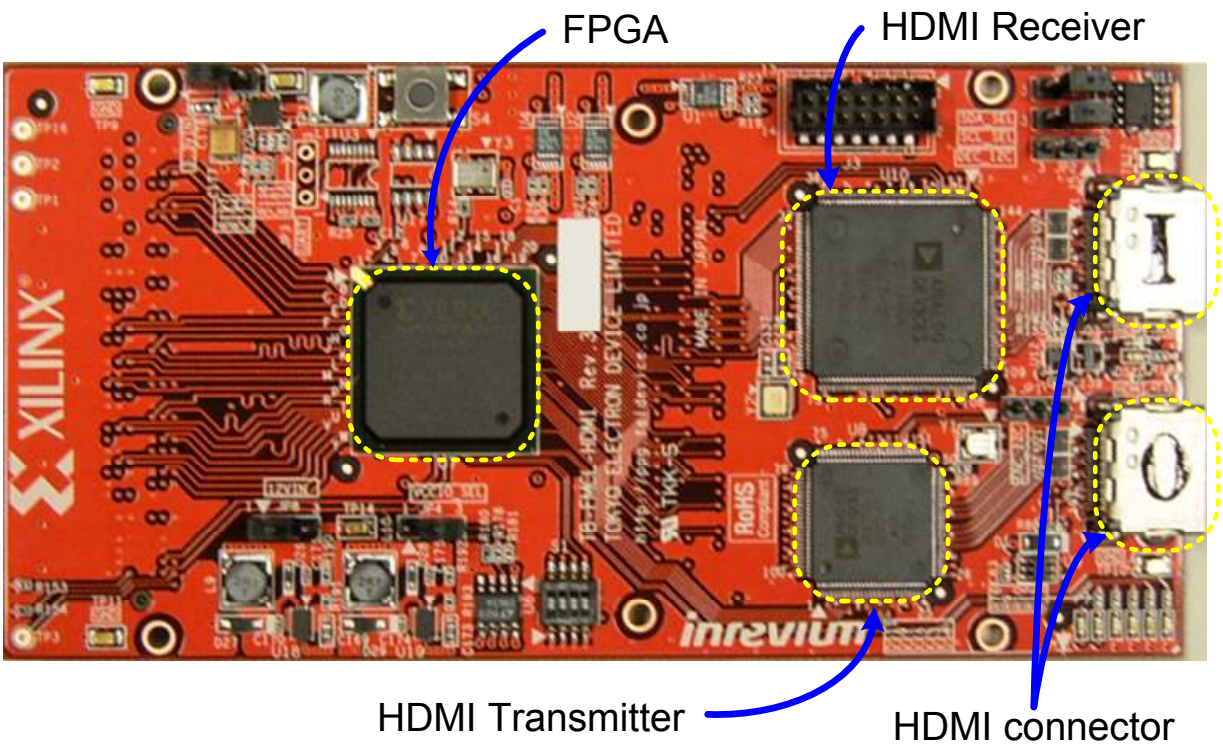

Figure 5-1 Component Side

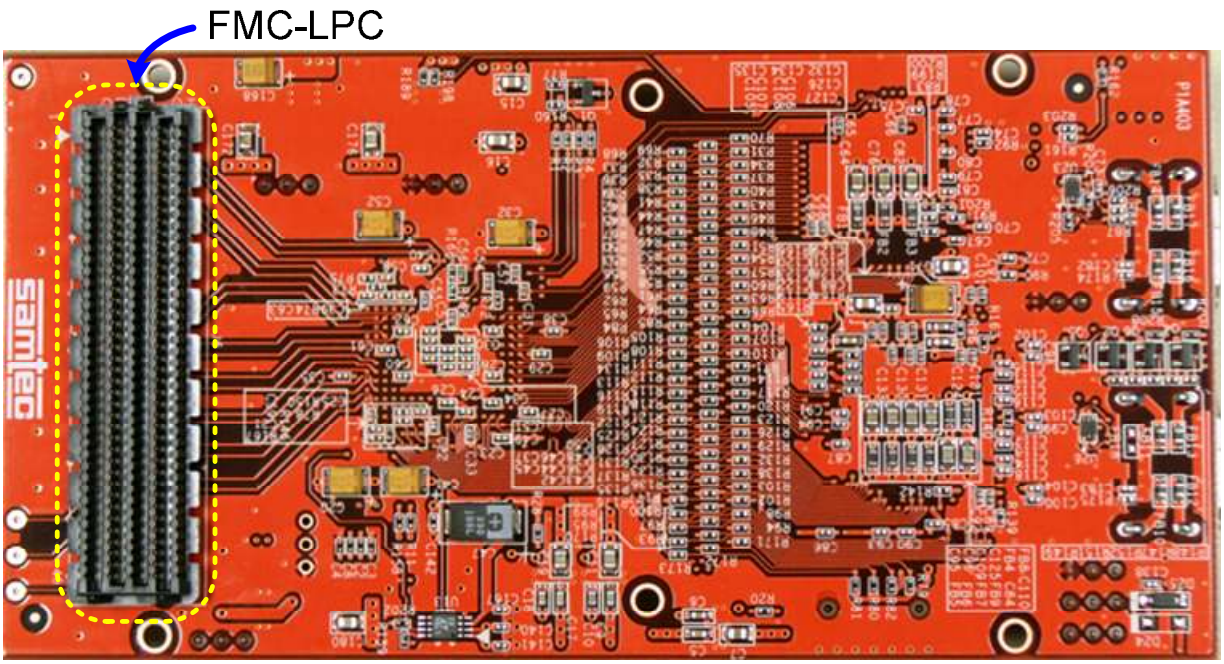

Figure 5-2 Solder Side

6. Board Specifications

The board specifications are as follows:

External Dimensions:	135.9 mm (W) x 69 mm (H)
Number of Layers:	8 layers
Board Thickness:	1.6 mm
Material:	FR-4
FPGA:	Xilinx XC3S400AN-5FGG400
FMC Connector:	Samtec ASP-134604-01
HDMI Connector:	Molex 5002541927

Following figure shows the board specifications. (Unit: mm)

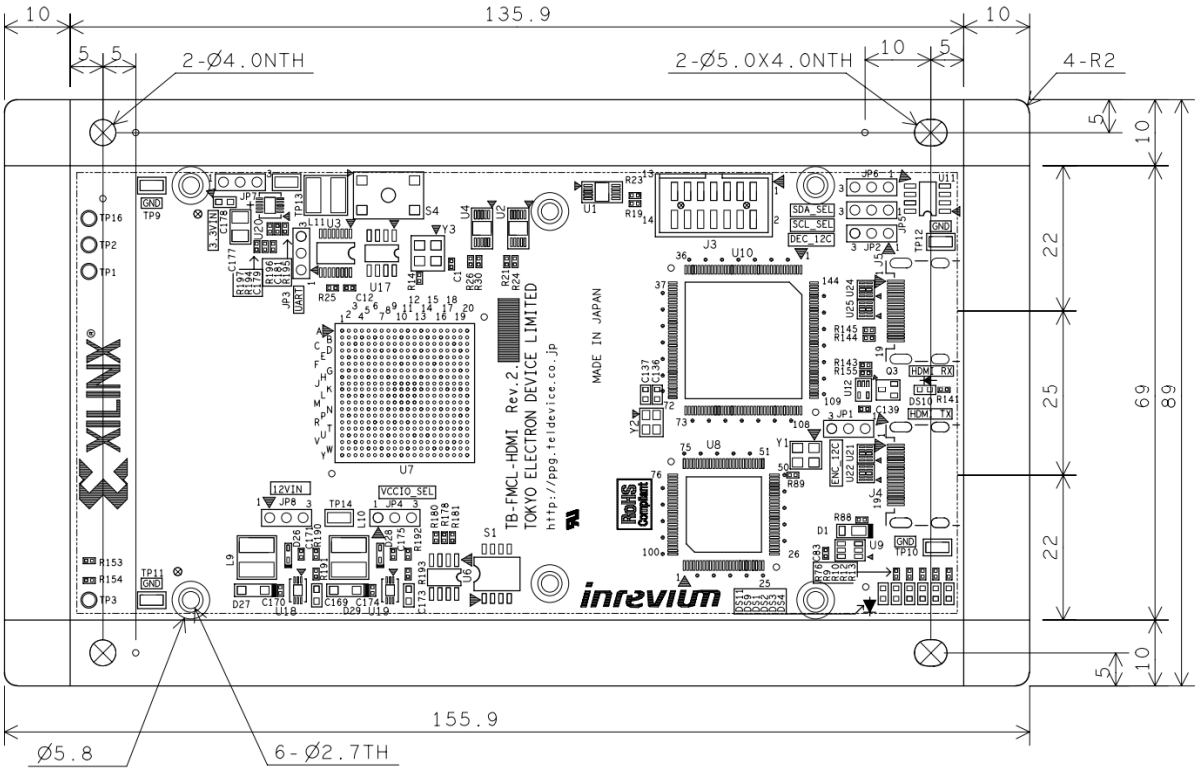

Figure 6-1 Board Dimensions (inclusive of wasteable substrate)

7. Description of Components

7.1. Power Supply Structure for the TB-FMCL-HDMI Board

Following figure shows the power supply structure for the board.

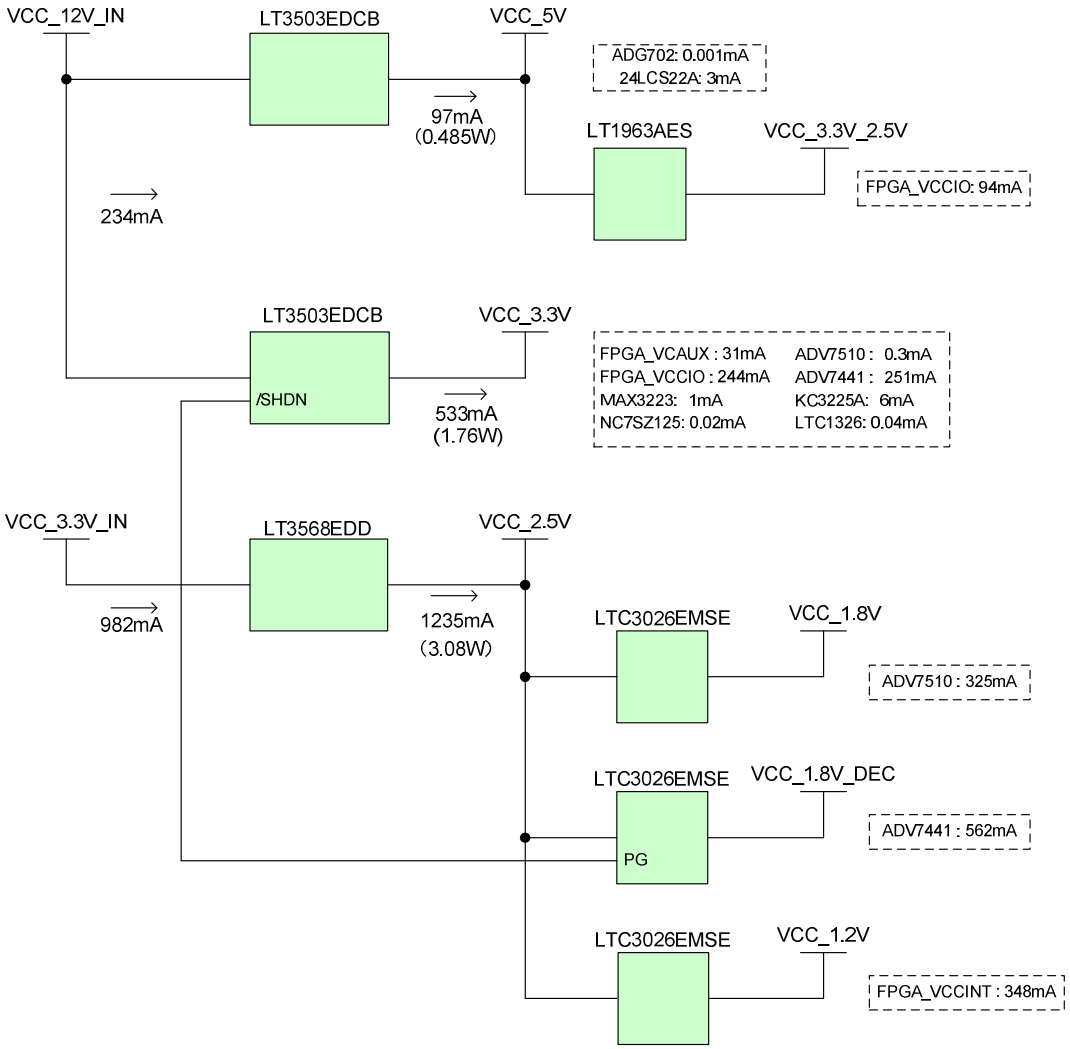

Figure 7-1 Power Supply Structure

VCC_3.3V_2.5V is used as the I/O voltage for FPGA BANK2/BANK3.
The BANK supports both 3.3V and 2.5V interfaces. The interface selection can be performed using JP4-VCCIO_SEL.

Caution: Initial setting, by jumper JP4, sets the FPGA IO standard at 2.5V (LVDS25). JP4 can provide 3.3V for FPGA IO power but the FPGA configuration ROM is 2.5V device. Please contact us if your application requires 3.3V IO.

Table 7-1 JP4-VCCIO_SEL Jumper Setting

No	IO Standard	Jumper Setting
1	3.3V	VCCIO_SEL: 1-2 Shorted
2	2.5V	VCCIO_SEL: 2-3 Shorted (default as shipped. Recommended setting.)

HDMI Transmitter block
The HDMI connector is the 5002541927 (Molex).
The HDMI transmitter device is the ADV7510BSTZ (Analog Devices).
The following EMI/ESD devices are used:
ESD: ESD Suppressor RCLAMP0524P (SEMTEC)
ESD: ESD Suppressor RCLAMP0504P (SEMTEC)

Following table shows the HDMI transmitter connector pin assignments.

Table 7-2 HDMI Connector (Transmit Side)

Pin #	Name	Description
1	TMDS DATA2+	TMDS Transmit Data 2+
2	TMDS SHLD2	TMDS Transmit Data 2 Shield
3	TMDS DATA2-	TMDS Transmit Data 2-
4	TMDS DATA1+	TMDS Transmit Data 1+
5	TMDS SHLD1	TMDS Transmit Data 1 Shield
6	TMDS DATA1-	TMDS Transmit Data 1-
7	TMDS DATA0+	TMDS Transmit Data 0+
8	TMDS SHLD0	TMDS Transmit Data 0 Shield
9	TMDS DATA0-	TMDS Transmit Data 0-
10	TMDS CLK+	TMDS Transmit Clock+
11	TMDS CLK SHLD	TMDS Transmit Clock Shield
12	TMDS CLK-	TMDS Transmit Clock-
13	CEC	CEC Signal
14	RESERVED	Reserved
15	DDC_SCL	DDC Serial Clock
16	DDC_SDA	DDC Serial Data
17	DDC/CEC GND	DDC/CEC Ground
18	DDC_+5V	+5V Power Supply
19	HOTPLUG_DET	Hot Plug Detection

HDMI Receiver block
The HDMI connector is the 5002541927 (Molex).
The HDMI Transmitter device is the ADV7441ABSTZ (Analog Devices).
The following EMI/ESD devices are used:
ESD: ESD Suppressor RCLAMP0524P (SEMTEC)
ESD: ESD Suppressor RCLAMP0504P (SEMTEC)

Following table shows the HDMI receiver connector pin assignments.

Table 7-3 HDMI Connector (Receiver Side)

Pin #	Name	Description
1	TMDS DATA2+	TMDS Receive Data 2+
2	TMDS SHLD2	TMDS Receiver Data 2 Shield
3	TMDS DATA2-	TMDS Receive Data 2-Shield
4	TMDS DATA1+	TMDS Receive Data 1+
5	TMDS SHLD1	TMDS Receive Data 1 Shield
6	TMDS DATA1-	TMDS Receive Data 1-
7	TMDS DATA0+	TMDS Receive Data 0+
8	TMDS SHLD0	TMDS Receive Data 0 Shield
9	TMDS DATA0-	TMDS Receive Data 0-
10	TMDS CLK+	TMDS Receive Clock+
11	TMDS CLK SHLD	TMDS Receive Clock Shield
12	TMDS CLK-	TMDS Receive Clock-
13	CEC	CEC Signal
14	RESERVED	Reserved
15	DDC_SCL	DDC Serial Clock
16	DDC_SDA	DDC Serial Data
17	DDC/CEC GND	DDC/CEC Ground
18	DDC_+5V	+5V Power Supply
19	HOTPLUG_DET	Hot Plug Detection

The receiver circuit has an EEPROM (Micro Chip: 24LCS22A-SN) containing the Extended Display Information Data (EDID) for the HDMI input channel.
The HDMI input/sink/receive connector's DDC_SCL and DDC_SDA are connected to jumper JP5-SCL/JP6-SDA to permit alternate sources of EDID data.
Table 7-4 describes the jumper JP5/JP6 settings which permit connection to either the EDID EEPROM or to the Transmit Device.

Caution: The EDID EEPROM contents are for evaluation purposes only and should not be shipped in a product to your end customer.

Table 7-4 JP5(SCL)/JP6(SDA) Jumper Setting

No	Access	Jumper Setting
1	To Transmitter	JP5(SCL): 2-3 Short JP6(SDA): 2-3 Short
2	To EEPROM	JP5(SCL): 1-2 Short JP6(SDA): 1-2 Short

7.2. FMC Connector

The FMC connector (Low-Pin Count), which is connected to the main board (or carrier card), uses a SAMTEC ASP-134604-01.
The TB-FMCL-HDMI board uses both the +12V and +3.3V rails supplied by the main board across the FMC connector.
An external power supply source can also be used when necessary for loop back testing.
Jumpers JP7 and JP8 select between FMC and external power sources.

Table 7-5 JP7/JP8 Jumper Setting

No	Power Supply	Jumper Setting
1	FMC Connector	JP7: 1-2 Short JP8: 1-2 Short
2	External Power Supply	JP7: 2-3 Short JP8: 2-3 Short

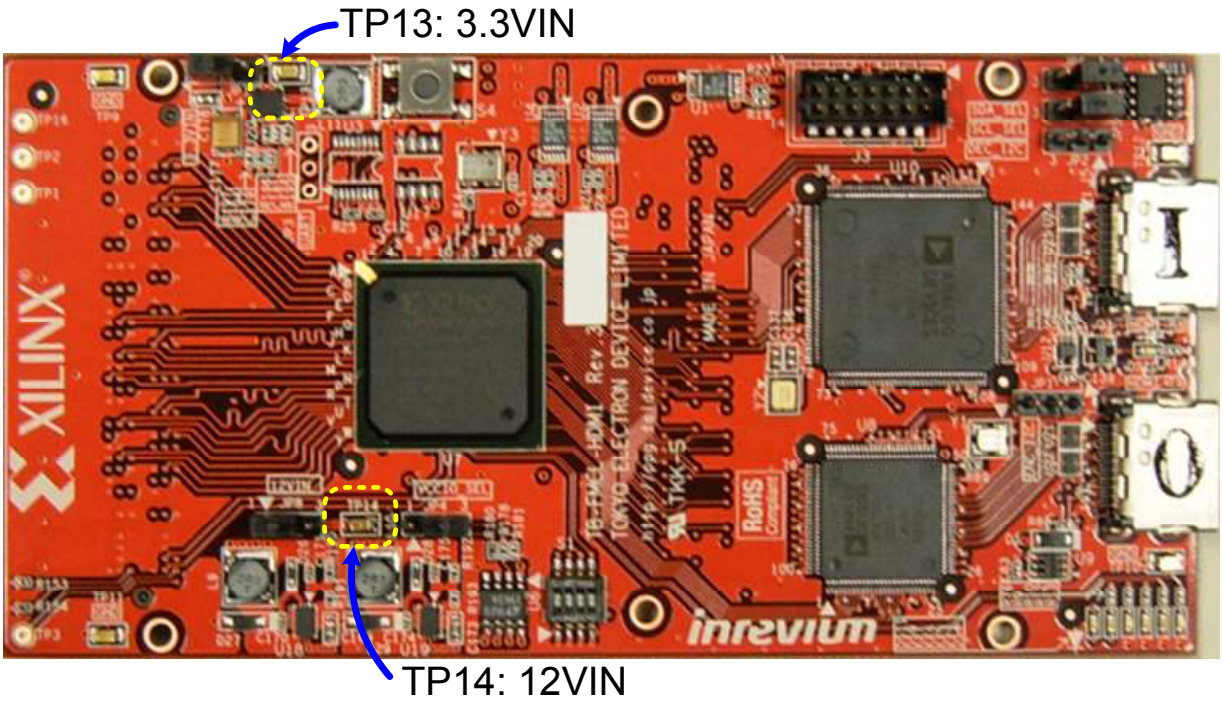

Figure 7-2 TP13, TP14 Location

Table 7-6 shows the FMC connector pin assignment.

Table 7-6 FMC Connector Pin Assignment

Pin #	C-row	D-row	G- row	H-row
1	GND	PG_C2M	GND	VREF_A_M2C
2	DP0_C2M_P	GND	CLK1_M2C_P	PRSNT_M2C_L
3	DP0_C2M_N	GND	CLK1_M2C_N	GND
4	GND	GBTCLK0_M2C_P	GND	CLK0_M2C_P
5	GND	GBTCLK0_M2C_N	GND	CLK0_M2C_N
6	DP0_M2C_P	GND	LA00_P_CC	GND
7	DP0_M2C_N	GND	LA00_N_CC	LA02_P
8	GND	LA01_P_CC	GND	LA02_N
9	GND	LA01_N_CC	LA03_P	GND
10	LA06_P	GND	LA03_N	LA04_P
11	LA06_N	LA05_P	GND	LA04_N
12	GND	LA05_N	LA08_P	GND
13	GND	GND	LA08_N	LA07_P
14	LA10_P	LA09_P	GND	LA07_N
15	LA10_N	LA09_N	LA12_P	GND
16	GND	GND	LA12_N	LA11_P
17	GND	LA13_P	GND	LA11_N
18	LA14_P	LA13_N	LA16_P	GND
19	LA14_N	GND	LA16_N	LA15_P
20	GND	LA17_P_CC	GND	LA15_N
21	GND	LA17_N_CC	LA20_P	GND
22	LA18_P_CC	GND	LA20_N	LA19_P
23	LA18_N_CC	LA23_P	GND	LA19_N
24	GND	LA23_N	LA22_P	GND
25	GND	GND	LA22_N	LA21_P
26	LA27_P	LA26_P	GND	LA21_N
27	LA27_N	LA26_N	LA25_P	GND
28	GND	GND	LA25_N	LA24_P
29	GND	TCK	GND	LA24_N
30	SCL	TDI	LA29_P	GND
31	SDA	TDO	LA29_N	LA28_P
32	GND	+3.3VAUX	GND	LA28_N
33	GND	TMS	LA31_P	GND
34	GA0	TRST	LA31_N	LA30_P
35	+12V	GA1	GND	LA30_N
36	GND	+3.3V	LA33_P	GND
37	+12V	GND	LA33_N	LA32_P
38	GND	+3.3V	GND	LA32_N
39	+3.3V	GND	VADJ	GND
40	GND	+3.3V	GND	VADJ

7.3. Other Interfaces

The board has the following interfaces.

7.3.1. JTAG Interface

The board has a JTAG connector to permit FPGA configuration by the user.

JTAG connector: 87832-1420 (Molex)

Table 7-7 JTAG Connector

Pin #	Signal	Pin #	Signal Name
1	GND	2	3.3V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	NC
13	GND	14	NC

7.3.2. General-Purpose Clock Interface

The board has a general-purpose clock oscillator (Kyocera KC5032C027.0000C30E00) which supplies a 27 MHz clock to the FPGA .

8. Status Display and Operation Functions

The board provides a variety of status display and operation functions using various LEDs and switches.

8.1.1. Display Function

The following table shows the onboard LEDs and their functions.

Table 8-1 LEDs

LED #	LED	Description
DS1	General-purpose LED1	Not used(always ON)
DS2	General-purpose LED2	Not used(always ON)
DS3	General-purpose LED3	Finish of write access of I2C
DS4	General-purpose LED4	Not used(always OFF)
DS9	Configuration status	ON: Configuration complete
DS11	HDMI transmit hot plug display	ON: Connected status
DS10	HDMI receiver hot plug display	ON: Connected status

8.1.2. Operation Function

Following table shows the onboard switches and their functions.

Table 8-2 Switches

Switch #	Function
S1-1	Color depth select (ON: 10bit, OFF: 8bit)
S1-2	Output setting (ON: DVI , OFF: HDMI)
S1-3	Input setting (ON: DVI , OFF: HDMI)
S1-4	Loopback connection select from receiver to transmitter. (ON: Receiver to Transmitter / OFF: Receiver to FMC, FMC to Transmitter)
S4	Reconfiguration pushbutton (Depress for greater then 3 seconds to initiate FPGA reconfiguration.)

Notice : Supported resolution
TV format (HDMI) : 480p(60frame),720p(50/60frame),1080i(30frame),1080p(60frame)
PC format (DVI) : UXGA(1600x1200@162MHz), WUXGA(1920x1200@154MHz)

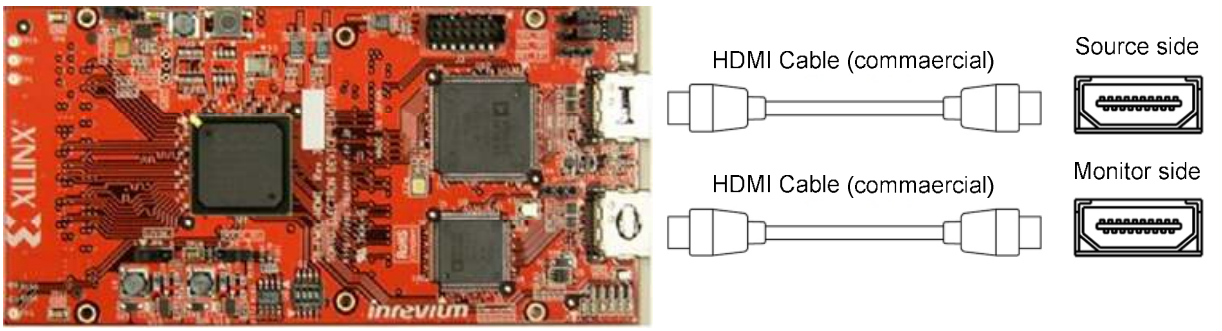

Figure 8-1 S1-2 OFF / S1-3 OFF : Cable connection

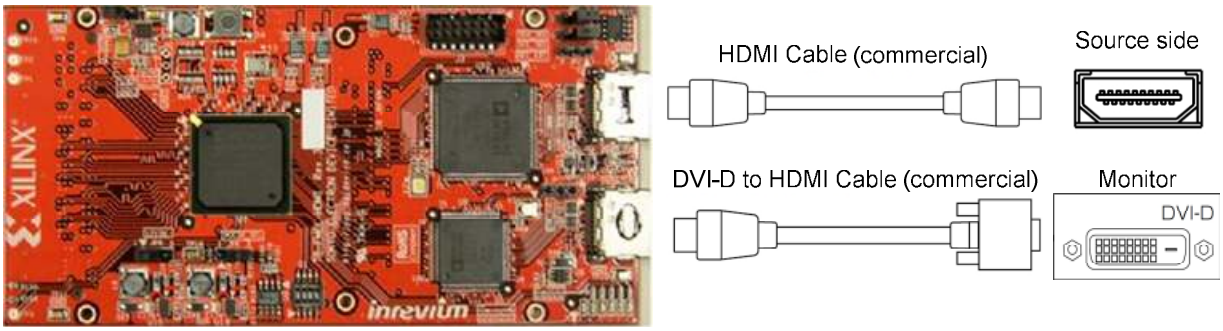

Figure 8-2 S1-2 ON / S1-3 OFF : Cable connection

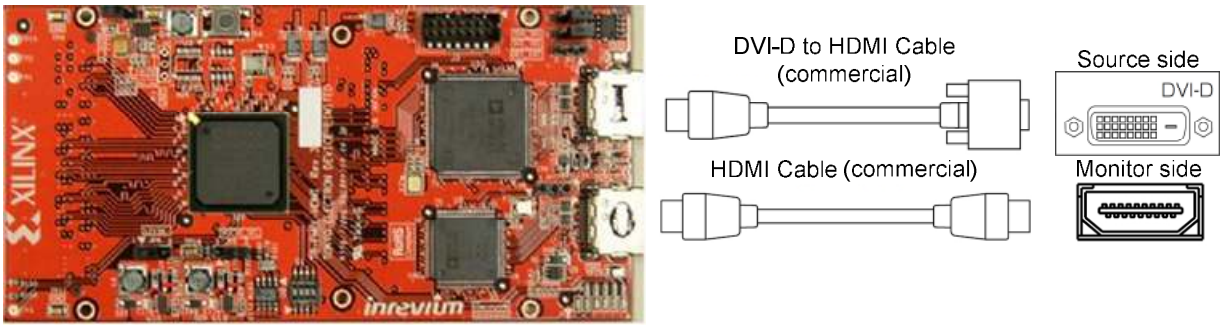

Figure 8-3 S1-2 OFF / S1-3 ON : Cable connection

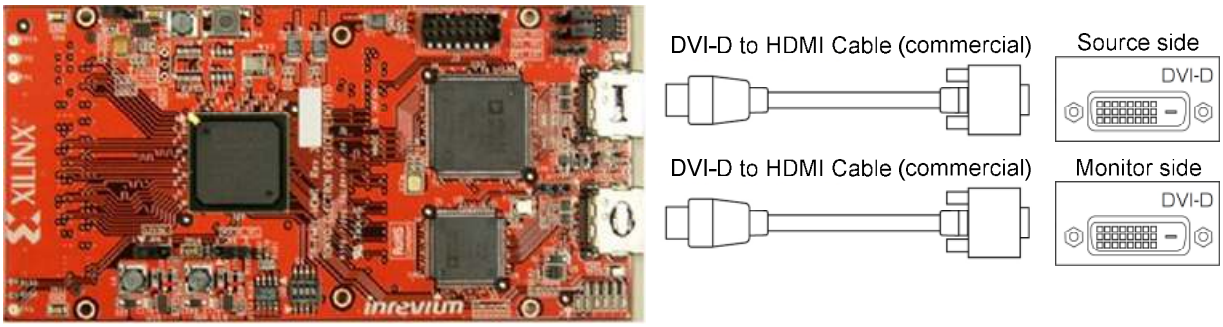

Figure 8-4 S1-2 ON / S1-3 ON : Cable connection

9. FPGA Pin Assignment

Table 9-1 shows the FPGA pin assignment.

The pin assignments between the FMC and FPGA signals are related by video signal format. When the HDMI input format is 8bits, the FPGA output signals are assigned to the most significant 8-bits and the least significant two bits of each color will be '0'.

Table 9-1 FPGA Pin Assignment

Pin Name	#	IO	Spec	Description
LA33_N	D3	IO	LVCMOS25	Not used
LA33_P	D4	IO	LVCMOS25	Not used
LA32_N	C2	IO	LVCMOS25	FMC to FPGA : DATA ENABLE
LA32_P	B1	IO	LVCMOS25	FPGA to FMC: DATA ENABLE
LA30_N	D2	IO	LVCMOS25	FMC to FPGA : VSYNC
LA30_P	C1	IO	LVCMOS25	FPGA to FMC : VSYNC
LA31_N	E1	IO	LVCMOS25	FMC to FPGA: HSYNC
LA31_P	D1	IO	LVCMOS25	FPGA to FMC : HSYNC
LA29_N	G5	IO	LVCMOS25	FMC to FPGA : DATA29(R9)
LA29_P	F4	IO	LVCMOS25	FPGA to FMC : DATA29(R9)
LA22_N	J5	IO	LVCMOS25	FMC to FPGA : DATA22(R2)
LA22_P	J6	IO	LVCMOS25	FPGA to FMC : DATA22(R2)
LA27_N	H4	IO	LVCMOS25	FMC to FPGA : DATA27(R7)
LA27_P	H6	IO	LVCMOS25	FPGA to FMC : DATA27(R7)
LA26_N	G4	IO	LVCMOS25	FMC to FPGA : DATA26(R6)
LA26_P	F3	IO	LVCMOS25	FPGA to FMC : DATA26(R6)
LA28_N	F2	IO	LVCMOS25	FMC to FPGA : DATA28(R8)
LA28_P	E3	IO	LVCMOS25	FPGA to FMC : DATA28(R8)
LA24_N	H2	IO	LVCMOS25	FMC to FPGA : DATA24(R4)
LA24_P	G3	IO	LVCMOS25	FPGA to FMC : DATA24(R4)
LA23_N	G1	IO	LVCMOS25	FMC to FPGA : DATA23(R3)
LA23_P	F1	IO	LVCMOS25	FPGA to FMC : DATA23(R3)
LA25_N	H3	IO	LVCMOS25	FMC to FPGA : DATA25(R5)
LA25_P	J4	IO	LVCMOS25	FPGA to FMC : DATA25(R5)
LA21_N	J2	IO	LVCMOS25	FMC to FPGA : DATA21(R1)
LA21_P	J3	IO	LVCMOS25	FPGA to FMC : DATA21(R1)
LA20_N	K2	IO	LVCMOS25	FMC to FPGA : DATA20(R0)
LA20_P	J1	IO	LVCMOS25	FPGA to FMC : DATA20(R0)
LA19_N	L3	IO	LVCMOS25	FMC to FPGA : DATA19(G9)
LA19_P	K3	IO	LVCMOS25	FPGA to FMC : DATA19(G9)
LA18_N_CC	L5	IO	LVCMOS25	FMC to FPGA : DATA18(G8)
LA18_P_CC	K4	IO	LVCMOS25	FPGA to FMC : DATA18(G8)
LA17_N_CC	M1	IO	LVCMOS25	FMC to FPGA : DATA17(G7)
LA17_P_CC	L1	IO	LVCMOS25	FPGA to FMC : DATA17(G7)
LA16_N	M3	IO	LVCMOS25	FMC to FPGA : DATA16(G6)
LA16_P	M2	IO	LVCMOS25	FPGA to FMC : DATA16(G6)

Pin Name	#	IO	Spec	Description
LA15_N	M5	IO	LVCMOS25	FMC to FPGA : DATA15(G5)
LA15_P	M4	IO	LVCMOS25	FPGA to FMC : DATA15(G5)
LA14_N	N2	IO	LVCMOS25	FMC to FPGA : DATA14(G4)
LA14_P	N1	IO	LVCMOS25	FPGA to FMC : DATA14(G4)
LA13_N	N4	IO	LVCMOS25	FMC to FPGA : DATA13(G3)
LA13_P	N3	IO	LVCMOS25	FPGA to FMC : DATA13(G3)
LA12_N	R1	IO	LVCMOS25	FMC to FPGA : DATA12(G2)
LA12_P	P1	IO	LVCMOS25	FPGA to FMC : DATA12(G2)
LA11_N	P4	IO	LVCMOS25	FMC to FPGA : DATA11(G1)
LA11_P	P3	IO	LVCMOS25	FPGA to FMC : DATA11(G1)
LA10_N	R3	IO	LVCMOS25	FMC to FPGA : DATA10(G0)
LA10_P	R2	IO	LVCMOS25	FPGA to FMC : DATA10(G0)
LA09_N	T2	IO	LVCMOS25	FMC to FPGA : DATA9(B9)
LA09_P	T1	IO	LVCMOS25	FPGA to FMC : DATA9(B9)
LA08_N	R4	IO	LVCMOS25	FMC to FPGA : DATA8(B8)
LA08_P	T3	IO	LVCMOS25	FPGA to FMC : DATA8(B8)
LA07_N	U3	IO	LVCMOS25	FMC to FPGA : DATA7(B7)
LA07_P	U1	IO	LVCMOS25	FPGA to FMC : DATA7(B7)
LA06_N	T4	IO	LVCMOS25	FMC to FPGA : DATA6(B6)
LA06_P	R5	IO	LVCMOS25	FPGA to FMC : DATA6(B6)
LA05_N	V2	IO	LVCMOS25	FMC to FPGA : DATA5(B5)
LA05_P	V1	IO	LVCMOS25	FPGA to FMC : DATA5(B5)
LA04_N	W2	IO	LVCMOS25	FMC to FPGA : DATA4(B4)
LA04_P	W1	IO	LVCMOS25	FPGA to FMC : DATA4(B4)
LA03_N	W4	IO	LVCMOS25	FMC to FPGA : DATA3(B3)
LA03_P	Y3	IO	LVCMOS25	FPGA to FMC : DATA3(B3)
LA02_N	R7	IO	LVCMOS25	FMC to FPGA : DATA2(B2)
LA02_P	T6	IO	LVCMOS25	FPGA to FMC : DATA2(B2)
LA01_N_CC	U5	IO	LVCMOS25	FMC to FPGA : DATA1(B1)
LA01_P_CC	V5	IO	LVCMOS25	FPGA to FMC : DATA1(B1)
LA00_N_CC	U6	IO	LVCMOS25	FMC to FPGA : DATA0(B0)
LA00_P_CC	T7	IO	LVCMOS25	FPGA to FMC : DATA0(B0)
CLK0_M2C_N	Y9	IO	LVCMOS25	Not used
CLK0_M2C_P	W9	IO	LVCMOS25	FMC to FPGA : Clock
CLK1_M2C_N	W10	IO	LVCMOS25	Not used
CLK1_M2C_P	V10	IO	LVCMOS25	FPGA to FMC : Clock
FMC_SCL	V11	IO	LVCMOS25	I2C serial clock
FMC_SDA	Y11	IO	LVCMOS25	I2C serial data
DSW0	R12	I	LVCMOS25	General-purpose DIP SW input 0
DSW1	T12	I	LVCMOS25	General-purpose DIP SW input 1
DSW2	Y12	I	LVCMOS25	General-purpose DIP SW input 2
DSW3	W13	I	LVCMOS25	General-purpose DIP SW input 3
DLED0	T15	O	LVCMOS25	General-purpose LED output 0
DLED1	U15	O	LVCMOS25	General-purpose LED output 1

Pin Name	#	IO	Spec	Description
DLED2	W16	O	LVCMOS25	General-purpose LED output 2
DLED3	Y16	O	LVCMOS25	General-purpose LED output 3
DEC_P29	A18	I	LVCMOS33	DEC Video data input 29
DEC_P28	B18	I	LVCMOS33	DEC Video data input 28
DEC_P27	C17	I	LVCMOS33	DEC Video data input 27
DEC_P26	D17	I	LVCMOS33	DEC Video data input 26
DEC_P25	E15	I	LVCMOS33	DEC Video data input 25
DEC_P24	D16	I	LVCMOS33	DEC Video data input 24
DEC_P23	A17	I	LVCMOS33	DEC Video data input 23
DEC_P22	B17	I	LVCMOS33	DEC Video data input 22
DEC_EXT_CLK	A16	O	LVCMOS33	DEC external clock output
DEC_P21	C16	I	LVCMOS33	DEC Video data input 21
DEC_P20	C15	I	LVCMOS33	DEC Video data input 20
DEC_P19	D15	I	LVCMOS33	DEC Video data input 19
DEC_P18	A14	I	LVCMOS33	DEC Video data input 18
DEC_P17	C14	I	LVCMOS33	DEC Video data input 17
DEC_P16	A15	I	LVCMOS33	DEC Video data input 16
DEC_P15	B15	I	LVCMOS33	DEC Video data input 15
DEC_P14	F13	I	LVCMOS33	DEC Video data input 14
DEC_P13	E13	I	LVCMOS33	DEC Video data input 13
DEC_P12	C13	I	LVCMOS33	DEC Video data input 12
DEC_P11	D14	I	LVCMOS33	DEC Video data input 11
DEC_P10	C12	I	LVCMOS33	DEC Video data input 10
DEC_P9	B13	I	LVCMOS33	DEC Video data input 9
DEC_P8	F12	I	LVCMOS33	DEC Video data input 8
DEC_P7	D12	I	LVCMOS33	DEC Video data input 7
DEC_P6	A12	I	LVCMOS33	DEC Video data input 6
DEC_P5	B12	I	LVCMOS33	DEC Video data input 5
DEC_P4	C11	I	LVCMOS33	DEC Video data input 4
DEC_P3	B11	I	LVCMOS33	DEC Video data input 3
DEC_LLC	D11	I	LVCMOS33	DEC LLC signal
SYSCLK_P	A10	I	LVCMOS33	System clock input (25MHz)
DEC_SCLK	D10	I	LVCMOS33	DEC Audio serial clock
DEC_MCLKOUT	A9	I	LVCMOS33	DEC Audio master clock
DEC_P2	C9	I	LVCMOS33	DEC Video data input 2
DEC_P1	B9	I	LVCMOS33	DEC Video data input 1
DEC_P0	C8	I	LVCMOS33	DEC Video data input 0
DEC_RESETX	B8	O	LVCMOS33	DEC reset output
DEC_INT2	D8	I	LVCMOS33	DEC interrupt input 2
DEC_INT1	C7	I	LVCMOS33	DEC interrupt input 1
DEC_VSYNC	F9	I	LVCMOS33	DEC VSYNC input
DEC_HSYNC	E9	I	LVCMOS33	DEC HSYNC input

Pin Name	#	IO	Spec	Description
DEC_DE	F8	I	LVCMOS33	DEC data enable
DEC_SCL	E8	O	LVCMOS33	DEC I2C serial clock
DEC_SDA	A7	IO	LVCMOS33	DEC I2C serial data
DEC_EXT_CLAMP	B7	O	LVCMOS33	DEC external CLAMP signal
DEC_LRCLK	C6	I	LVCMOS33	DEC LRCLK signal
DEC_I2S3	A6	I	LVCMOS33	DEC I2S Audio signal 3
DEC_I2S2	B5	I	LVCMOS33	DEC I2S Audio signal 2
DEC_I2S1	A5	I	LVCMOS33	DEC I2S Audio signal 1
DEC_I2S0	F7	I	LVCMOS33	DEC I2S Audio signal 0
DEC_SPDIF	E7	I	LVCMOS33	DEC SPDIF digital Audio input
DEC_DDCA_SDA_F	D6	IO	LVCMOS33	DEC slave serial data
DEC_DDCA_SCL_F	C5	I	LVCMOS33	DEC slave serial clock
DEC_CEC	C4	IO	LVCMOS33	DEC CEC signal
DEC_HPD_IO	A4	O	LVCMOS33	DEC hot plug control
DEC_DET1	B3	I	LVCMOS33	DEC Detect signal
UART_TXD	A3	O	LVCMOS33	UART transmit data *Not used
UART_RXD	F6	I	LVCMOS33	UART receive data *Not used
EEPROM_SCL	E6	O	LVCMOS33	EEPROM serial clock *Not used
EEPROM_SDA	A2	IO	LVCMOS33	EEPROM serial data *Not used
ENC_HPD_IO	V20	O	LVCMOS33	ENC hot plug control
ENC_PD	W20	O	LVCMOS33	ENC power down signal
ENC_LRCLK	U18	O	LVCMOS33	ENC LRCLK signal
ENC_SCLK	V19	O	LVCMOS33	ENC Audio serial clock
ENC_I2S3	T17	O	LVCMOS33	ENC I2S Audio signal 3
ENC_I2S2	T20	O	LVCMOS33	ENC I2S Audio signal 2
ENC_I2S1	T18	O	LVCMOS33	ENC I2S Audio signal 1
ENC_I2S0	U20	O	LVCMOS33	ENC I2S Audio signal 0
ENC_MCLK	U19	O	LVCMOS33	ENC Audio master clock
ENC_SPDIF	P17	O	LVCMOS33	ENC SPDIF digital Audio output
ENC_DSD_CLK	P16	O	LVCMOS33	ENC DSD clock
ENC_DSD5	R17	O	LVCMOS33	ENC DSD Audio data 5
ENC_DSD4	R18	O	LVCMOS33	ENC DSD Audio data 4
ENC_DSD3	R20	O	LVCMOS33	ENC DSD Audio data 3
ENC_DSD2	R19	O	LVCMOS33	ENC DSD Audio data 2
ENC_DSD1	P20	O	LVCMOS33	ENC DSD Audio data 1
ENC_DSD0	P18	O	LVCMOS33	ENC DSD Audio data 0
ENC_VSYNC	N17	O	LVCMOS33	ENC VSYNC output
ENC_HSYNC	N15	O	LVCMOS33	ENC HSYNC output
ENC_DE	N19	O	LVCMOS33	ENC data enable
ENC_D0	N18	O	LVCMOS33	ENC Video data output 0
ENC_D1	M18	O	LVCMOS33	ENC Video data output 1
ENC_D2	M17	O	LVCMOS33	ENC Video data output 2

Pin Name	#	IO	Spec	Description
ENC_D3	L16	O	LVCMOS33	ENC Video data output 3
ENC_D4	L15	O	LVCMOS33	ENC Video data output 4
ENC_D5	M20	O	LVCMOS33	ENC Video data output 5
ENC_D6	M19	O	LVCMOS33	ENC Video data output 6
ENC_D7	L18	O	LVCMOS33	ENC Video data output 7
ENC_D8	L19	O	LVCMOS33	ENC Video data output 8
ENC_D9	L17	O	LVCMOS33	ENC Video data output 9
ENC_D10	K18	O	LVCMOS33	ENC Video data output 10
ENC_D11	J20	O	LVCMOS33	ENC Video data output 11
ENC_D12	K20	O	LVCMOS33	ENC Video data output 12
ENC_D13	J18	O	LVCMOS33	ENC Video data output 13
ENC_D14	J19	O	LVCMOS33	ENC Video data output 14
ENC_D15	K16	O	LVCMOS33	ENC Video data output 15
ENC_D16	J17	O	LVCMOS33	ENC Video data output 16
ENC_DCLK	H18	O	LVCMOS33	ENC Video data clock
ENC_D17	H19	O	LVCMOS33	ENC Video data output 17
ENC_D18	G20	O	LVCMOS33	ENC Video data output 18
ENC_D19	H20	O	LVCMOS33	ENC Video data output 19
ENC_D20	H17	O	LVCMOS33	ENC Video data output 20
ENC_D21	G18	O	LVCMOS33	ENC Video data output 21
ENC_D22	F19	O	LVCMOS33	ENC Video data output 22
ENC_D23	F20	O	LVCMOS33	ENC Video data output 23
ENC_D24	F18	O	LVCMOS33	ENC Video data output 24
ENC_D25	G17	O	LVCMOS33	ENC Video data output 25
ENC_D26	E19	O	LVCMOS33	ENC Video data output 26
ENC_D27	E20	O	LVCMOS33	ENC Video data output 27
ENC_D28	F17	O	LVCMOS33	ENC Video data output 28
ENC_D29	E18	O	LVCMOS33	ENC Video data output 29
ENC_D30	D18	O	LVCMOS33	ENC Video data output 30
ENC_D31	D20	O	LVCMOS33	ENC Video data output 31
ENC_D32	F16	O	LVCMOS33	ENC Video data output 32
ENC_D33	G16	O	LVCMOS33	ENC Video data output 33
ENC_D34	C19	O	LVCMOS33	ENC Video data output 34
ENC_D35	C20	O	LVCMOS33	ENC Video data output 35
ENC_SDA	B19	IO	LVCMOS33	ENC I2C serial data
ENC_SCL	B20	O	LVCMOS33	ENC I2C serial clock
ENC_CEC	N14	IO	LVCMOS33	ENC CEC signal
ENC_INT	P15	I	LVCMOS33	ENC interrupt input

10. Carrier Card FPGA Interface

The following figure shows timing waveforms of the signaling interface between the carrier board FPGA and the TB-6S-FMCL-HDMI mezzanine FPGA. .
Both interfaces are source synchronous and rising edge clocked.

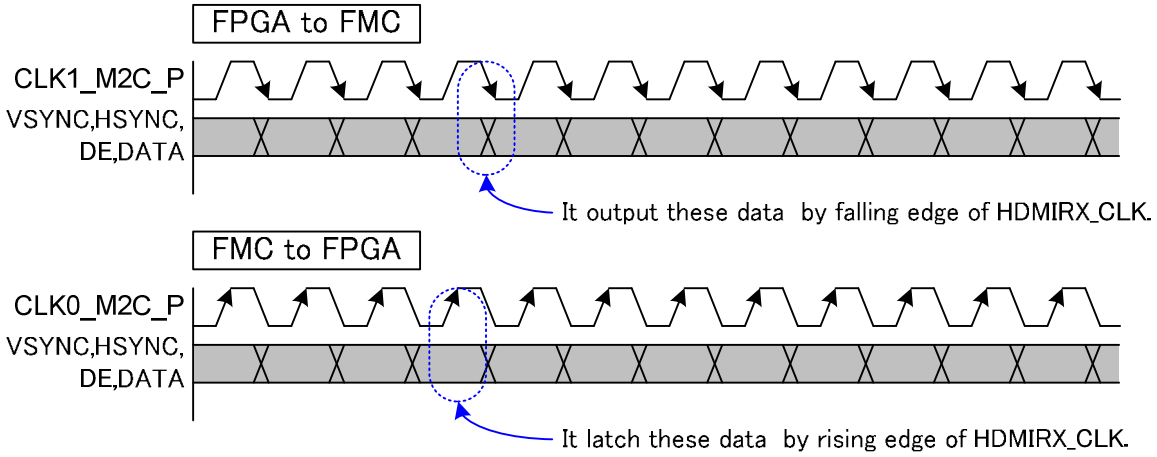

Figure 10-1 Timing of input and output signals

11. Default Switch Settings

Following figure shows default switch settings (see yellow-dotted circles).

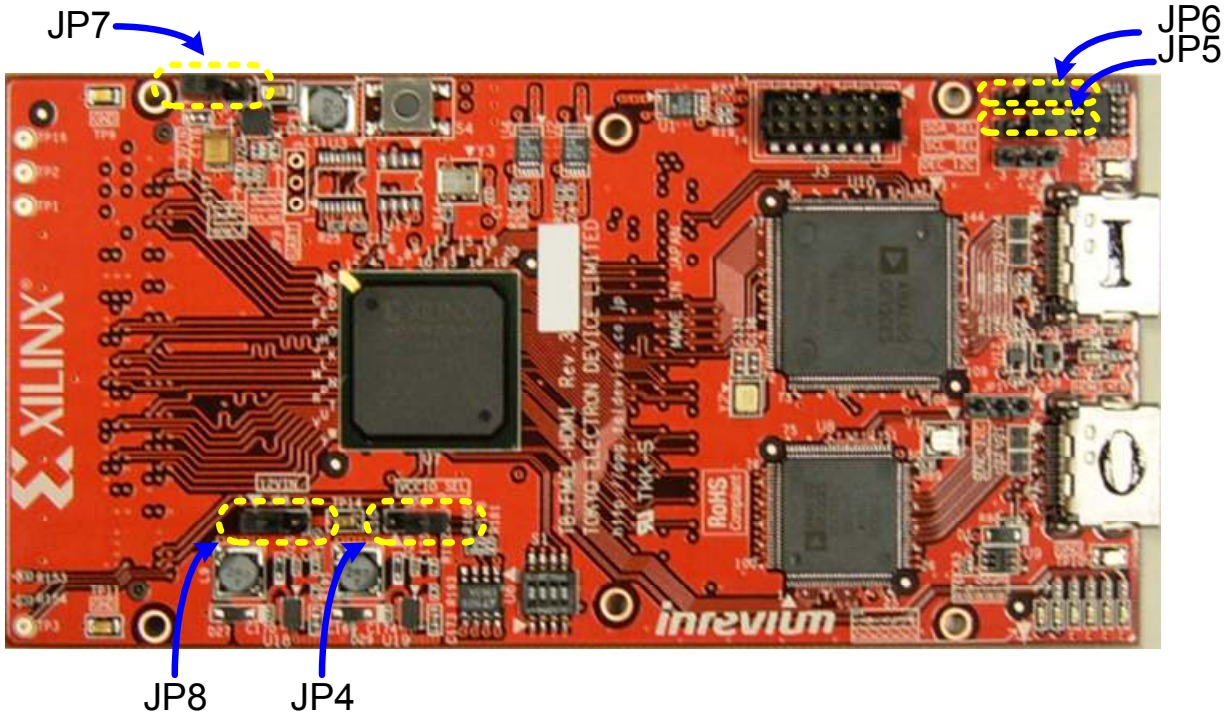

Figure 11-1 Default Switch Settings (Component Side)

Table 11-1 Default Jumper Settings

Silk No.	Initial Setting	Function
JP4	2-3 short	VCCIO_SEL (1-2: 3.3V / 2-3: 2.5V)
JP5	1-2 short	SCL_SEL (1-2: HDMI / 2-3: FPGA)
JP6	1-2 short	SDA_SEL (1-2: HDMI/ 2-3: FPGA)
JP7	1-2 short	3.3VIN_SEL (1-2: FMC connector / 2-3: External power supply)
JP8	1-2 short	12VIN_SEL (1-2: FMC connector / 2-3: External power supply)

Table 11-2 Default DIP Switch Settings

Silk No.	Initial Setting	Function
SW1-1	OFF	Color depth select for receiver and transmitter (ON: 10bit / OFF: 8bit)
SW1-2	OFF	Output setting (ON: DVI / OFF: HDMI)
SW1-3	OFF	Input setting (ON: DVI / OFF: HDMI)
SW1-4	OFF	External loopback connection select from Receiver to Transmitter. (ON: Receiver to Transmitter loopback) (OFF: Receiver to FMC, FMC to Transmitter – no loopback, normal operation)

12. Example of Use

Figure 12-1 show an example of use when the loop back path is enabled by jumper selection.
Please be careful with onboard jumper settings!

If video is not see at the HDMI TX output, press pushbutton S4 longer than 3 seconds to force a re-configuration of the TB-FMCL-HDMI FPGA.

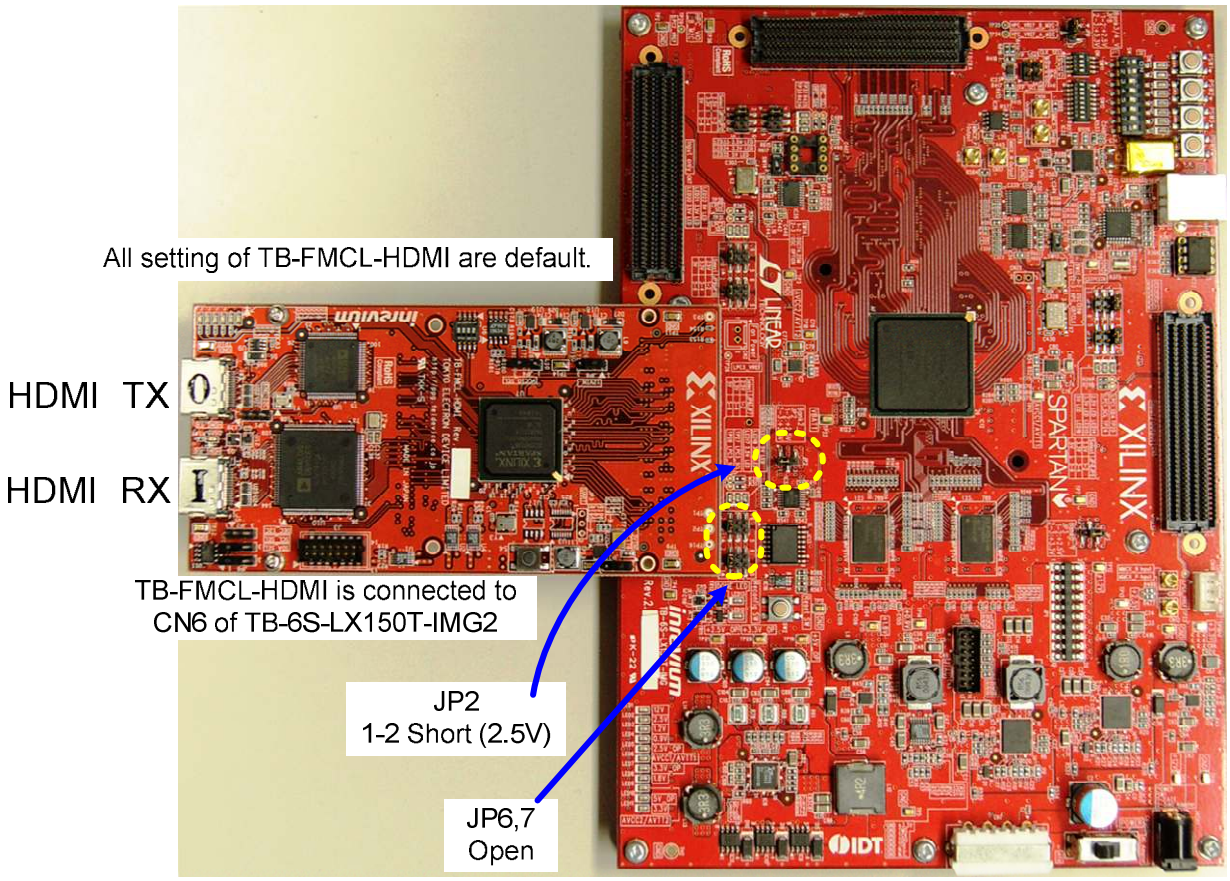

Figure 12-1 Example of Use

Table 12-1 Jumper Settings in the Example

No.	Silk No.	Setting	Function
1	JP2	1-2	Bank2 IO voltage setting (**2.5V** / 3.3V)
2	JP6,7	Open	FMC3 VADJ voltage setting (2.5V / 3.3V / 5V / **None**) (The two jumper settings must always be in the same relative positions).

* The values indicated by boldface are used in the example above.

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